REMARKS

Claims 1, 6 – 9 and 17 are pending and under consideration in the above-identified application.

In the Office Action, Claims 1, 6 – 9 and 17 were rejected.

In this Amendment, Claims 1 and 17 are amended. No new matter has been introduced as a result of this Amendment.

Accordingly, Claims 1, 6 – 9 and 17 remain at issue.

I. 35 U.S.C. § 103 Obviousness Rejection of Claims

Claims 1, 7 – 9 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ota et al. ("Ota") (JP 2002-163624) in view of Kodai (U.S. Patent No. 5,026,452). Although Applicants respectfully traverse this claim rejection, Claim 1 has been amended to clarify the invention and remove any ambiguities that may have been at the basis of this rejection.

Claim 1 is directed to an IC card comprising an IC module which comprises an IC chip mounted on an insulating substrate having an antenna coil, a sealing material which encapsulates the IC chip, and a chip reinforcing plate provided on at least an IC mounted surface of the insulating substrate and formed on the IC chip through the sealing material; and a core layer comprising a plurality of sheet materials having the IC module disposed therebetween, wherein, in the plurality of sheet materials, at least the sheet materials adjacent to the IC module have a through hole (a) for containing therein the IC chip the sealing material and the chip reinforcing plate, and (b) formed to penetrate the adjacent sheet materials in a region corresponding to an IC mounted portion of the IC module before placing the IC chip therein, the plurality of sheet materials constituting the core layer comprise at least a pair of inner core sheets adjacent to the IC module, a relationship of $(B1 + C1) - 20\ \mu m \leq A \leq (B1 + C1) + 10\ \mu m$ is satisfied, where A (μm) represents the sum of heights of the through holes, B1 (μm) represents a projection height on an IC mounted surface of the IC module, and C1 (μm) represents a projection height on an IC non-mounted surface of the IC module, the relationships $B = B1 \pm 30\ \mu m$, and $C = C1 \pm 30\ \mu m$ are satisfied, wherein B (μm) represents a height of the through hole on the side of the IC mounted surface of the IC module, and C (μm) represents a height of the through hole on the side of the IC non-mounted surface of the IC module, and the through holes are larger than at

least one of a length and a width of said sealing material and *than at least one of a length and a width of* said chip reinforcing plate *so as to form at least one empty region in said through holes.*

Referring to Applicants' FIGs. 6 - 8, as illustrative examples, Applicants' claimed invention comprises inner core sheets S2, S3 which have, respectively, through holes S2c, S3b provided in portions corresponding to the respective chip mounted portions of the IC module 11. The through holes S2c, S3b are formed so that they are larger than the individual outer diameters of the sealing resins 15, 17 and reinforcing plates 16, 18 provided on the IC mounted portion of the IC module 11, and, when the inner core sheets S2, S3 are individually stacked on the IC module 11, the through hole S3b contains therein the IC chip 14, the sealing resin 15, and the reinforcing plate 16 and the through hole S2c contains therein the sealing resin 17 and the reinforcing plate 18.

In contrast, both Ota and Kodai fail to teach or suggest through holes that are larger than at least one of a length and a width of said sealing material and than at least one of a length and a width of said chip reinforcing plate so as to form at least one empty region in said through holes. As shown, in FIGs. 1 – 4 and 7 – 8 of Ota, the reinforcing plates 9 and 9' and the closure resin 7 and 7' fill completely their corresponding through holes formed in sheets 15 and 16. No empty region is formed in Ota's through holes. In addition, as shown in FIGs. 1 – 8B of Kodai, the IC module 2 fills completely the trough holes 7. Thus, similarly to Ota, no empty region is formed in Kodai's through holes. As such, Ota and Kodai, taken singly or in combination with each other, fail to teach or suggest all of the limitations of Claim 1.

Thus, Claim 1 is patentable over Ota in view of Kodai, as are dependent Claims 7 – 9 for at least the same reasons.

Claim 17, which has been amended to recite the same distinguishable limitation as that of Claim 1, is therefore patentable over Ota and Kodai.

Accordingly, Applicants respectfully request that these 35 U.S.C. § 103 claim rejections be withdrawn.

II. 35 U.S.C. § 103 Obviousness Rejection of Claims

Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ota et al. or Kodai et al in view of Saito et al. ("Saito") (JP 11-0278324). Applicants respectfully traverse this rejection.

Claim 6 is dependent on Claim 1 shown above to be patentable over Ota and Kodai. Moreover, in addition to Ota and Kodai, Saito also fails to teach or suggest that the through holes of an IC card are larger than at least one of a length and a width of the sealing material and than at least one of a length and a width of said chip reinforcing plate so as to form at least one empty region in said through holes. As such, Claim 1 is patentable over Ota Kodai and Saito, taken singly or in combination with each other, as is dependent Claim 6 for at least the same reasons.

Accordingly, Applicants respectfully request that these 35 U.S.C. § 103 claim rejections be withdrawn.

III. Conclusion

In view of the above amendments and remarks, Applicant submits that Claims 1, 6 – 9 and 17 are clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect.

Respectfully submitted,

Dated: Sept 26, 2007 By: David R Metzger

David R. Metzger
Registration No. 32,919
SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. Box 061080
Wacker Drive Station, Sears Tower
Chicago, Illinois 60606-1080
(312) 876-8000